REMARKS

Applicant thanks the examiner for the courtesy extended to Applicant's representatives Lawrence Cullen and Yoshinobu Idogawa during a interview on November 10, 2004.

During the interview, Applicant advised the Examiner that several claims would be cancelled to be placed in a divisional application. Applicant also explained the invention in claims 80 and above and the Matsuzaki reference. Particularly, Applicant explained that Matsuzaki discloses either sign bit or 0 bit expansion according to the type of operation to be performed, rather than according to a designation of a register unit. It is Applicant's understanding that the Examiner appreciated the distinctions.

I. Introduction

Claims 80-94 are pending in the above application.

Claims 80-94 stand rejected under 36 U.S.C. §102.

II. Amendments

Claims 1-79 have been cancelled without prejudice or disclaimer. Applicant reserves the right to file a divisional application on claims 1-79.

Claims 80, 83, 85, 88, 91 and 94 have been amended to be in better grammatical form and/or to remove any possibility of being interpreted as containing mean plus function terminology.

The amendments to the claims have been made with respect to the original patent claims as set forth by MPEP 1453. For the Examiner's convenience, a marked up version of the claims compared to the previous version are attached in the appendix.

No new matter has been added.

III. Prior Art Rejections

Claims 80-94 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuzaki et al. (U.S. Pat. 5,440,701) (hereafter "Matsuzaki").

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference as arranged in the claim. See, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986); *Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983).

Matsuzaki does not disclose a processor which has a first register, a second register, a zero-extending unit, and a sign extending unit, wherein the zero-extending unit zero-extends data when the instruction designates the first register unit and the sign-extending unit sign-extends data when the instruction designates the second register unit, as required by amended claim 80. Independent claims 83, 85, 88, 91, and 94 also each contain limitations directed toward performing either sign extension or zero extension according to a designation of a register. Matsuzaki discloses either sign bit or 0 bit expansion according to the type of operation to be performed. Col. 4: 57-68.

Accordingly, as Matsuzaki does not disclose each and every limitation of claims 80, 83, 85, 88, 91, and 94, Matsuzaki does not anticipate claims 80, 83, 85, 88, 91, and 94. As dependent claims contain all of the limitations of their base claims, claims 81, 82, 84, 86, 86, 89 92 and 93 also are not anticipated by Matsuzaki.

IV. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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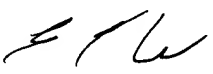

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